GDDR5 SDRAM

H5GQ2H24AFR

The GDDR5 SGRAM is a high speed dynamic random access memory designed for applications requiring high bandwidth. GDDR5 devices contain the following number of bits: 2Gb has 2,147,483,648 bits and sixteen banks The GDDR5 SGRAM uses a 8n prefetch architecture and DDR interface to achieve high speed operation. The device can be configured to operate in x32 mode or x16 (clamshell) mode. The mode is detected during device initialization. The GDDR5 interface transfers two 32 bit wide data words per WCK clock cycle to/from the I/O pins. Corresponding to the 8n prefetch a single write or read access consists of a 256bit wide, two CK clock cycle data transfer at the internal memory core and eight corresponding 32bit wide one half WCK clock cycle data transfers at the I/O pins. The GDDR5 SGRAM operates from a differential clock CK and CK#. Commands are registered at every rising edge of CK. Addresses are registered at every rising edge of CK and every rising edge of CK#. GDDR5 replaces the pulsed strobes (WDQS & RDQS) used in previous DRAMs such as GDDR4 with a free running differential forwarded clock (WCK/WCK#) with both input and output data registered and driven respectively at both edges of the forwarded WCK. Read and write accesses to the GDDR5 SGRAM are burst oriented; an access starts at a selected location and consists of a total of eight data words. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command and the next rising CK# edge are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command and the next rising CK# edge are used to select the bank and the column location for the burst access.

Features

Single ended interface for data, address and command
Quarter datarate differential clock inputs CK/CK# for ADR/CMD
Two half datarate differential clock inputs WCK/ WCK#, each associated with two data bytes (DQ, DBI#, EDC)
Double Data Rate (DDR) data (WCK)
Single Data Rate (SDR) command (CK)
Double Data Rate (DDR) addressing (CK)
16 internal banks
4 bank groups for tCCDL = 3 tCK
8n prefetch architecture: 256 bit per array read or write access
Burst length: 8 only
Programmable CAS latency: 5 to 20 tCK
Programmable WRITE latency: 1 to 7 tCK
WRITE Data mask function via address bus (single/ double byte mask)
Data bus inversion (DBI) & address bus inversion (ABI)
Input/output PLL on/off mode
Address training: address input monitoring by DQ pins
WCK2CK clock training with phase information by EDC pins
Data read and write training via READ FIFO
READ FIFO pattern preload by LDFF command
Direct write data load to READ FIFO by WRTR command
Consecutive read of READ FIFO by RDTR command
Read/Write data transmission integrity secured by cyclic redundancy check (CRC8)
READ/WRITE EDC on/off mode
Programmable EDC hold pattern for CDR
Programmable CRC READ latency = 0 to 3 tCK
Programmable CRC WRITE latency = 7 to 14 tCK
Low Power modes
RDQS mode on EDC pin
Optional onchip with readout
Auto & self refresh modes
Auto precharge option for each burst access
32ms, auto refresh (16k cycles)
controlled self refresh rate
Ondie termination (ODT); nominal values of 60 ohm and 120 ohm
Pseudo open drain (POD15) compatible outputs (40 ohm pulldown, 60 ohm pullup)
ODT and output drive strength autocalibration with external resistor ZQ pin (120 ohm)
Programmable termination and driver strength offsets
Selectable external or internal VREF for data inputs; programmable offsets for internal VREF
Separate external VREF for address / command inputs
Vendor ID, FIFO depth and Density info fields for identification
x32/x16 mode configuration set at powerup with EDC pin
Mirror function with MF pin
Boundary scan function with SEN pin
1.6V / 1.5V / 1.35V +/ (3%xVDD)V supply for device operation (VDD)
1.6V / 1.5V / 1.35V +/ (3%xVDDQ)V supply for I/O interface (VDDQ)
170 ball BGA package

Ordering Information

Part No	Power Supply	WCK Frequency	Max Data Rate	Interface
*H5GQ2H24AFR-R2C	VDD/VDDQ = 1.6	3.50GHz	7.0Gbps/pin	POD_15
H5GQ2H24AFR-R0C	VDD/VDDQ = 1.5	3.00GHz	6.0Gbps/pin	POD_15
	VDD/VDDQ = 1.35V	2.50GHz	5.0Gbps/pin	POD_135
H5GQ2H24AFR-T2C	VDD/VDDQ = 1.5	2.50GHz	5.0Gbps/pin	POD_15
	VDD/VDDQ = 1.35	2.00GHz	4.0Gbps/pin	POD_135
H5GQ2H24AFR-T0C	VDD/VDDQ = 1.5	2.00GHz	4.0Gbps/pin	POD_15

Note1) Above Hynix P/N's are Lead-free, RoHS Compliant and Halogen-free
Note2) 7Gbps(-R2C) is guaranteed in the condition of Bank Grouping On (Either 8 Bank Groups or 4 Bank Groups)